

## REMARKS

Claims 1-52 are pending in the Application, all of which stand rejected by the Office Action having a mailing date of March 20, 2009. Claims 1, 6, 28, and 49 are amended by the present response. Claims 1, 6, 28, and 49 are independent claims, while claims 2-5, 7-27, 29-48, and 50-52 depend either directly or indirectly from independent claims 1, 6, 28, and 49, respectively.

Applicant respectfully requests reconsideration of claims 1-52, in light of the following remarks.

### Rejection of Claims Under 35 U.S.C. §112

Claims 25, 26, 46, and 47 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office Action asserts that "it is not clear how the 'one processor' can comprise a plurality of processors." (See Office Action at p. 6.)

Further explaining the rejection, the Office Action states:

At page 13, first paragraph, Applicant submits that the language of claims 25, 26 and 46 is not indefinite, but is clear and definite. However, the Examiner respectfully disagrees. As the Applicant admitted, "at least one processor (i.e. one or more) comprises a plurality of processors (i.e. more than one)" [emphasis added] (Remarks, last line of page 12), it is clear that "at least one processor" has two situations either comprises one processor or more. For the case that only has one processor, it is unclear how the "one processor" can comprise a plurality of processors. Therefore the 35 U.S.C. § 112 rejection to claims 25, 26, 46 and 47 is maintained.

(Office Action at p. 2-3.) Applicant respectfully traverses these rejections. The language of the at issue claims does not present any case in which only one processor

somehow comprises a plurality of processors. Claim 25 explicitly recites "a plurality of processors" and therefore expressly excludes the purported case of only one processor. Similarly, claims 26, 46, and 47 expressly recite "a plurality of processors" and also therefore expressly exclude the purported case of only one processor. The case of "only one processor" is expressly excluded from these dependent claims. Further still, at no point does the claim language state that "only one processor" comprises a plurality of processors. Instead, the claim language merely narrows a range recited in the independent claim from which it depends – "at least one" (i.e. one or more) in the independent claim is narrowed to "a plurality" (i.e. two or more) in the dependent claim.

Each of these claims merely recites a range that is narrower than the range recited in the independent claim from which it depends. Applicant recognizes that use of a narrow numerical range that falls within a broader range in the same claim may, in some circumstances, render the claim indefinite if stated in a single claim. (See MPEP § 2173.05(c).) However, the MPEP expressly provides that "[a] narrower range or preferred embodiment may also be set forth in another independent claim or in a dependent claim." (*Id.*) Here, each of claims 25, 26, 46, and 47 sets forth a narrower range (i.e. these claims recite that the range comprises "a plurality..." so these claims claim a range of 2 or more) than the claim from which it depends (which recites "at least one..." so the independent claims claim a range of 1 or more). Each of claims 25, 26, 46, and 47 does not claim 2 ranges (or somehow claim only one processor), but instead only claims one range (2 or more) which is narrower than the range for the claim from which it depends (1 or more). The MPEP specifically provides that "it is not improper under 35 U.S.C. 112, second paragraph, to present a dependent claim that sets forth a narrower range for an element than the range set forth in the claim from which it depends." (*Id.*) Applicant respectfully submits that a range of a "plurality" (i.e. two or more) is a narrower range than "at least one" (i.e. one or more), and that the claims presently at issue present dependent claims that set forth a narrower range for the "at least one processor" element than the range set forth in the independent claims from which they depend. As such, these claims are not improper under 35 U.S.C. § 112. (See MPEP § 2173.05(c).) Applicant respectfully submits that claims 25, 26, 46, and 47

are allowable under 35 U.S.C. § 112 and respectfully requests withdrawal of those rejections.

### **Rejection of Claims Under 35 U.S.C. §103(a)**

Claims 1-24 and 32 were rejected under 35 U.S.C. §102(a) as being unpatentable over Patrick J. O'Neil, WO 02/41147 A1 (hereinafter "O'Neil") in view of James S. Woodward (US Patent No. 6,148,441, hereinafter "Woodward"). Applicant respectfully traverses these rejections, for at least the reasons set forth in previous submissions.

Further, the independent claims of the present application have been amended to further clarify certain patentably distinct aspects of the presently claimed subject matter. For example, claim 1 has been amended to clarify that the method claimed by claim 1 includes, *inter alia*, "identifying, from a group corresponding to memory devices to which access has been enabled, updating software corresponding to at least the associated type of the at least one of the plurality of memory devices" and "wherein the non-volatile memory comprises software functions enabling access to and manipulation of the first memory device and the second memory device, first updating software corresponding to the first associated type, and second updating software corresponding to the second associated type." Additional support for this amendment may be found in the specification at, for example, ¶¶ [0072]-[0073]. Applicant respectfully submits that the cited art, either alone or in combination, does not teach, suggest, or otherwise render obvious at least these aspects of the presently claimed subject matter.

Applicant appreciates the Office Action's recognition that "O'Neil does not explicitly disclose identifying the associated type of the memory devices." (See Office Action at p. 7.) However, the Office Action asserts that Woodward "discloses a method for determining the type of flash memory being used (see for example, col.8, lines 16-41)." (See *id.*) While Applicant respectfully traverses the assertions, as also discussed in previous submissions, nevertheless claim 1 is amended by the present response to further clarify patentable distinctiveness from the cited art. The cited portion of Woodward (namely, 8:16-41) reads as follows:

As part of the installation procedure for the new Interrupt 15, and as shown in step 104, the CPU determines whether the flash ROM used in the PC system is an INTEL® device or an ADVANCED MICRO DEVICES® flash ROM. According to the preferred embodiment, the CPU performs this operation by checking if the flash ROM is a 5 volt device. If it is, the CPU considers it an AMD flash ROM device and continues on to step 108. If, conversely, the CPU decides that the flash ROM is not a 5 volt device, then the CPU deems it to be a 12 volt INTEL® flash ROM and exits from the program in step 106.

In step 108, the CPU retrieves the "old" Interrupt 15 routine and saves it for the end of the "new" Interrupt 15 routine (i.e., the "old" routine is tacked onto the end of the "new" routine). The CPU in step 110 then sets the address for the Interrupt 15 in the interrupt vector table equal to the location of the "new" Interrupt 15, that preferably comprises the subroutine of FIG. 4B. In step 112, the CPU determines how much space the program of the present invention will occupy by subtracting the beginning address of the program from the end address. The CPU performs a TSR (terminate and stay resident) operation in step 114 and informs the operating system of the address of the "new" Interrupt 15 and the amount of space occupied by that routine, so that the operating system will not attempt to take that space in memory.

Applicant respectfully submits that this portion of Woodward teaches, at most, identifying only whether or not a given flash ROM is a 5 volt device (and then simply assumes it to be an AMD device, or if not, an Intel device), and does not teach, suggest, or otherwise render obvious, for example, "identifying, from a group corresponding to memory devices to which access has been enabled, updating software corresponding to at least the associated type of the at least one of the plurality of memory devices" as claimed. Applicant respectfully submits that the cited art does not teach a group of updating software corresponding to memory devices to which access has been enabled, let alone identifying from a group as claimed. In fact, Woodward teaches "exit[ing] from the program" if the flash ROM is "deem[ed] to be a 12 volt INTEL® flash ROM" (*see* Woodward at 8:23-26), and would therefore teach against the presently claimed subject matter. (*See also id.* at 6:19-21: "The present invention is designed for

use in a PC system implementing flash ROM devices in which, unlike the Intel flash ROM,..." (emphasis added)). Thus, the cited disclosure does not teach the first and second memory devices to which access has been enabled and identifying updating software from a group as claimed, and instead teaches against the presently claimed subject matter. In any event, Applicant respectfully submits that Woodward, either alone or in combination with the other cited art, does not teach, suggest, or otherwise render obvious "identifying, from a group corresponding to memory devices to which access has been enabled, updating software corresponding to at least the associated type of the at least one of the plurality of memory devices" and "wherein the non-volatile memory comprises software functions enabling access to and manipulation of the first memory device and the second memory device, first updating software corresponding to the first associated type, and second updating software corresponding to the second associated type" as claimed.

As discussed above and in previous submissions as well, Applicant respectfully submits that the proposed combination of O'Neill and Woodward does not render obvious independent claim 1 or claims 2-5 which depend from independent claim 1. Accordingly, Applicant respectfully requests that the rejection of claims 1-5 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Turning to independent claim 6 and its dependent claims, Applicant respectfully submits that claim 6 is amended by the present response to recite limitations similar to certain aspects discussed above of independent claim 1, and is therefore similarly allowable. Therefore, Applicant respectfully submits that independent claim 6, and any claims that depend therefrom, are allowable over the cited art, for similar reasons.

Applicant now turns to claim 28 and claims dependent therefrom. Claims 28-31 and 33-45 were rejected under 35 U.S.C. §103(a) as being unpatentable over O'Neill. Applicant respectfully traverses the rejection. The Office Action states, at page 24:

Claims 28-31 and 33-45 are network/system version for performing the claimed method as in claims 6-9 and 11-24 addressed above, wherein all claimed limitation functions have been addressed and/or set forth above and certainly a computer system would need to run and/or practice such

function steps disclosed by reference above. Thus, they also would have been obvious.

Thus, the Office Action rejects claims 28-31 and 33-45 for similar reasons set forth for the rejection of claim 6-9 and 11-24, and fails to identify any additional basis or supporting teachings for the instant rejection beyond those set forth in the rejection of claim 6-9 and 11-24. Similar to the above discussion, independent claim 28 is amended to recite, *inter alia*, "an update agent employing a memory library to interact with the plurality of memory devices in non-volatile memory in the electronic device and to identify, from a group corresponding to memory devices to which access has been enabled, updating software corresponding to at least an associated type of at least one of the plurality of memory devices." As discussed above, O'Neill in combination with Woodward fails to teach, suggest or otherwise render obvious at least that aspect of the presently claimed subject matter. As such, Applicant respectfully submits that O'Neill standing alone would also fail to render claims 28-31 and 33-45 unpatentable as well, for at least similar reasons as discussed above. Accordingly, Applicant respectfully requests that the rejection of claims 28-31 and 33-45 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Claims 25-27, 46-49, 51, and 52 were rejected under 35 U.S.C. §103(a) as being unpatentable over O'Neill in view of Gove *et al.* (US 5,471,592, hereinafter "Gove"). Applicant respectfully traverses the rejection. Nevertheless, independent claim 49 is amended by the present response to recite certain of the aspects also discussed above in connection with the previously discussed independent claims.

Beginning with claims 25-27 and 46-48, claims 25-27 depend from claim 6, and claims 46-48 depend from claim 28. As discussed above, Applicant respectfully submits that claims 6 and 28 are allowable over the cited art, and that Gove fails to overcome the deficiencies of O'Neill, set forth above. Because claims 6 and 28 are allowable over the proposed combination of references, Applicant respectfully submits that claims 25-27 and 46-48 that depend therefrom are also allowable, for at least the same reasons.

Turning to independent claim 49, as an initial matter, Applicant respectfully submits that the "plurality of memory units (chips)" asserted by the Office Action do not teach, suggest, or otherwise render obvious the plurality of flash memory chips comprising a first flash memory chip and a second flash memory chip having associated types that are not the same, as claimed (and, as discussed in the previous submission, the Office Action does not provide the required articulation of how the cited art purportedly renders claim 49 obvious). In any event, as mentioned above, claim 49 is amended by the present response to recite certain of the aspects discussed above in connection with the other independent claims. Applicant respectfully submits that claim 49 and its dependent claims are allowable for similar reasons to those discussed above.

Therefore, for at least the reasons set forth above, Applicant respectfully requests that the rejection of claims 25-27, 46-49, 51, and 52 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

Claim 50 was rejected under 35 U.S.C. §103(a) as being unpatentable over O'Neill in view of Gove, and further in view of Woodward. Claim 50 depends from independent claim 49, discussed above. Applicant respectfully submits that claim 49 is also allowable over the proposed combination of references, and that Woodward fails to remedy the deficiencies of O'Neill and Gove, set forth above. Accordingly, Applicant respectfully requests that the rejection of claim 50 under 35 U.S.C. §103(a) be reconsidered and withdrawn.

## Conclusion

In general, the Office Action makes various statements regarding the pending claims and the cited references that are now moot in light of the above. Thus, Applicant will not address such statements at the present time. However, Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant believes that all of the pending claims are in condition for allowance. Should the Examiner disagree or have any questions regarding this submission, the Applicant invites the Examiner to contact the undersigned at (312) 775-8000 for an interview.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

Date: June 22, 2009

/Kevin E. Borg/  
Kevin E. Borg  
Reg. No. 51,486

Hewlett-Packard Company  
Intellectual Property Administration  
Legal Department, M/S 35  
P.O. Box 272400  
Fort Collins, CO 80527-2400